NEXCOMM asia

GSI TECHNOLOGY

Founded in 1995, GSI Technology, Inc. is a leading provider of high performance semiconductor memory solutions for military, medical, automotive and other applications.

"SigmaQuad SRAMs are synchronous memories with separate Read and Write data buses. "Quad" refers to their ability to transfer 4 beats of data (2 beats per data bus) in a single clock cycle."

Military Temperature SRAMs

SigmaQuad-IVe™ SRAMs

144Mb SigmaQuad-IVe (Package - 260 BGA)

GSI P/N	Config	Speed (MHz)	Voltage	Features
GS81314LD36GK-120M GS81314LD18GK-120M	4M x 36 8M x 18	1200	V_{DD}—1.25 ~ 1.3 V V_{DDQ}—1.2 ~ 1.3 V HSTL I/O	SigmaQuad-ive Burst of 4 Read Latency=6 On-Die Termination Option Muti-Bank, ECCRAM™
GS81314LQ36GK-120M GS81314LQ18GK-120M	4M x 36 8M x 18	1200	V_{DD}—1.25 ~ 1.3 V V_{DDQ}—1.2 ~ 1.3 V HSTL I/O	SigmaQuad-IVe Burst of 2 Read Latency = 6 On-Die Termination Option Multi-Bank, ECCRAM™
GS81314LD37GK-800M GS81314LD19GK-800M	4M x 36 8M x 18	800	V_{DD}—1.3 V V_{DDQ}—1.2 ~ 1.3 V HSTL I/O	SigmaQuad-IVe Burst of 4 Read Latency = 5 On-Die Termination Option Single-Bank, ECCRAM™
GS81314LQ37GK-800M GS81314LQ18GK-800M	4M x 36 8M x 18	800	V_{DD}—1.3 V V_{DDQ}—1.2 ~ 1.3 V HSTL I/O	SigmaQuad-IVe Burst of 2 Read Latency = 5 On-Die Termination Option Single-Bank, ECCRAM™

SigmaQuad-IIIe™ SRAMs

288Mb SigmaQuad-IIIe (Package - 260 BGA)

GSI P/N	Config	Speed (MHz)	Voltage	Features
GS82583ED36GK-625M GS82583ED18GK-625M	8M x 36 16M x 18	625	V_{DD}—1.3 V V_{DDQ}—1.2V/1.3 V/1.5 V	SigmaQuad-IIIe Burst of 4 Read Latency = 3 On-Die Termination Option
GS82583EQ36GK-450M GS82583EQ18GK-450M	8M x 36 16M x 18	450	V_{DD}—1.3 V V_{DDQ}—1.2V/1.3 V/1.5 V	SigmaQuad-IIIe Burst of 2 Read Latency = 3 On-Die Termination Option

144Mb SigmaQuad-IIIe (Package - 260 BGA)

GSI P/N	Config	Speed (MHz)	Voltage	Features
GS81313LD36GK-714M GS81313LD18GK-714M	4M x 36 8M x 18	714	V_{DD}—1.25 ~ 1.3 V V_{DDQ}—1.2 ~ 1.3 V HSTL I/O	SigmaQuad-IIIe Burst of 4 Read Latency = 3 On-Die Termination Option ECCRAM™
GS81313LQ36GK-714M GS81313LQ18GK-714M	4M x 36 8M x 18	714	V_{DD}—1.25 ~ 1.3 V V_{DDQ}—1.2 ~ 1.3 V HSTL I/O	SigmaQuad-IIIe Burst of 2 Read Latency = 3 On-Die Termination Option ECCRAM™

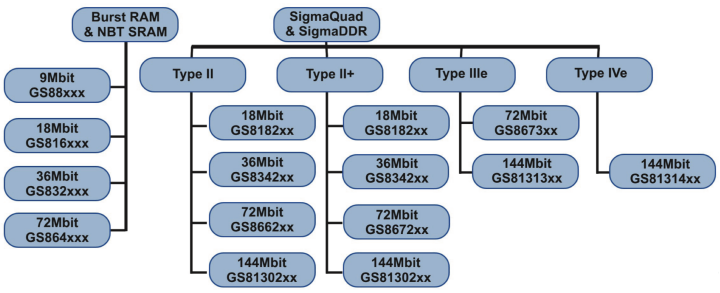
72Mb SigmaQuad-IIIe (Package - 260 BGA)

GSI P/N	Config	Speed (MHz)	Voltage	Features
GS8673ED36BK-625M GS8673ED18BK-625M	2M x 36 4M x 18	625	V_{DD}—1.35 V V_{DDQ}—1.2 V/1.5 V	SigmaQuad-IIIe Burst of 4 Read Latency = 3 On-Die Termination Option ECCRAM™
GS8673EQ36BK-625M GS8673EQ18BK-625M	2M x 36 4M x 18	625	V_{DD}—1.35 V V_{DDQ}—1.2 V/1.5 V	SigmaQuad-IIIe Burst of 2 Read Latency = 3 On-Die Termination Option ECCRAM™

SigmaQuad-IITM and SigmaQuad-II+TM SRAMs

144Mb SigmaQuad-II+ (Package - 165 BGA (15x17mm))

GSI P/N	Config	Speed (MHz)	Voltage	Features
GS81302D38E-450M GS81302D20E-450M GS81302D11E-450M GS81302D06E-450M	4M x 36 8M x 18 16M x 9 16M x 8	450	V_{DD}—1.8 V V_{DDQ}—1.5 V/1.8 V	SigmaQuad-II+ Burst of 4 Read Latency = 2.5 On-Die Termination Option
GS81302Q37E-300M GS81302Q19E-300M GS81302Q10E-300M GS81302Q07E-300M	4M x 36 8M x 18 6M x 9 16M x 8	300	V_{DD}—1.8 V V_{DDQ}—1.5 V/1.8 V	SigmaQuad-II+ Burst of 2 Read Latency = 2. On-Die Termination Option



144Mb SigmaQuad-II (Package - 165 BGA (15x17mm))

GSI P/N	Config	Speed (MHz)	Voltage	Features
GS81302D36E-350M GS81302D18E-350M GS81302D09E-350M GS81302D08E-350M	4M x 36 8M x 18 16M x 9 16M x 8	350	V_{DD}—1.8 V V_{DDQ}—1.5 V/1.8 V	SigmaQuad-II Burst of 4
GS81302Q36E-250M GS81302Q18E-250M GS81302Q09E-250M GS81302Q08E-250M	4M x 36 8M x 18 16M x 9 16M x 8	250	V_{DD}—1.8 V V_{DDQ}—1.5 V/1.8 V	SigmaQuad-II Burst of 2

72Mb SigmaQuad-II+ (Package - 165 BGA (13x15 mm))

GSI P/N	Config	Speed (MHz)	Voltage	Features
GS8662D38BD-450M GS8662D20BD-450M GS8662D11BD-450M GS8662D06BD-450M	2M x 36 4M x 18 8M x 9 8M x 8	450	V_{DD}—1.8 V V_{DDQ}—1.5 V/1.8 V	SigmaQuad-II+ Burst of 4 Read Latency = 2.5 On-Die Termination Option
GS8662Q37BD-333M GS8662Q19BD-333M GS8662Q10BD-333M GS8662Q07BD-333M	2M x 36 4M x 18 8M x 9 8M x 8	333	V_{DD}—1.8 V V_{DDQ}—1.5 V/1.8 V	SigmaQuad-II+ Burst of 2 Read Latency = 2.0 On-Die Termination Option

72Mb SigmaQuad-II (Package - 165 BGA (13x15 mm))

GSI P/N	Config	Speed (MHz)	Voltage	Features
GS8662D36BD-350M GS8662D18BD-350M GS8662D09BD-350M GS8662D08BD-350M	2M x 36 4M x 18 8M x 9 8M x 8	350	V_{DD}—1.8 V V_{DDQ}—1.5 V/1.8 V	SigmaQuad-II Burst of 4
GS8662Q36BD-333M GS8662Q18BD-333M GS8662Q09BD-333M GS8662Q08BD-333M	2M x 36 4M x 18 8M x 9 8M x 8	333	V_{DD}—1.8 V V_{DDQ}—1.5 V/1.8 V	SigmaQuad-II Burst of 2

36Mb SigmaQuad-II+ (Package - 165 BGA (13x15 mm))

GSI P/N	Config	Speed (MHz)	Voltage	Features
GS8342D38BD-500M GS8342D20BD-500M GS8342D11BD-500M GS8342D06BD-500M	1M x 36 2M x 18 4M x 9 4M x 8	500	V_{DD}—1.8 V V_{DDQ}—1.5 V/1.8 V	SigmaQuad-II+ Burst of 4 Read Latency = 2.5 On-Die Termination Option
GS8342Q37BD-300M GS8342Q19BD-300M GS8342Q10BD-300M GS8342Q07BD-300M	1M x 36 2M x 18 4M x 9 4M x 8	300	V_{DD}—1.8 V V_{DDQ}—1.5 V/1.8 V	SigmaQuad-II+ Burst of 2 Read Latency = 2.0 On-Die Termination Option

36Mb SigmaQuad-II (Package - 165 BGA (13x15 mm))

GSI P/N	Config	Speed (MHz)	Voltage	Features
GS8342D36BD-350M GS8342D18BD-350M GS8342D09BD-350M GS8342D08BD-350M	1M x 36 2M x 18 4M x 9 4M x 8	350	V_{DD}—1.8 V V_{DDQ}—1.5 V/1.8 V	SigmaQuad-II+ Burst of 4
GS8342Q36BD-333M GS8342Q18BD-333M GS8342Q09BD-333M GS8342Q08BD-333M	1M x 36 2M x 18 4M x 9 4M x 8	333	V_{DD}—1.8 V V_{DDQ}—1.5 V/1.8 V	SigmaQuad-II+ Burst of 2

18Mb SigmaQuad-II+ (Package - 165 BGA (13x15 mm))

GSI P/N	Config	Speed (MHz)	Voltage	Features
GS8182D37BD-400M GS8182D19BD-400M	512K x 36 1M x 18	400	V_{DD}—1.8 V V_{DDQ}—1.5 V/1.8 V	SigmaQuad-II+ Burst of 4 Read Latency = 2.0

18Mb SigmaQuad-II (Package - 165 BGA (13x15 mm))

GSI P/N	Config	Speed (MHz)	Voltage	Features
GS8182D36BD-375M GS8182D18BD-375M GS8182D09BD-375M GS8182D08BD-375M	512K x 36 1M x 18 2M x 9 2M x 8	375	V_{DD}—1.8 V V_{DDQ}—1.5 V/1.8 V	SigmaQuad-II Burst of 4
GS8182Q36BD-300M GS8182Q18BD-300M GS8182Q09BD-300M GS8182Q08BD-300M	512K x 36 1M x 18 2M x 9 2M x 8	300	V_{DD}—1.8 V V_{DDQ}—1.5 V/1.8 V	SigmaQuad-II Burst of 2

SigmaQuad-II/II+

Desc.	Burst Size	Read Latency	Ordering Information				
			18Mb	36Mb	72Mb	144Mb	288Mb
Quad Data Rate	2	1.5.2.0. 2.5.3**	GS8182Q	GS8342Q	GS8662Q GS8672Q*	GS81302Q	GS82582Q
	4		GS8182D	GS8342D	GS8662D GS8672D*	GS81302D	GS82582D

* On-chip ECC for aditional SER protection
** RL =3 for 288Mb Quad B4 only.

SigmaQuad-IIIe

Desc.	Burst Size	Read Latency	Operating Frequency	Ordering Information		
				72Mb	144Mb	288Mb
Quad Data Rate	2	3	Up to 800 MHz	GS8673EQ	GS81313LQ GS81313HQ	GS82583EQ
	4	3	Up to 833 MHz	GS86&3ED	GS81313LD GS81313HD	GS82583ED

SigmaQuad-IVe

Desc.	Burst Size	Read Latency	Operating Frequency	Ordering Information
				144Mb (x18, x36)
Quad Data Rate	2	6	Up to 1333 MHz	GS81314LQ GS81314PQ
	4	6	Up to 1333 MHz	GS81314LD GS81314PD

SigmaQuad-II+ Memory Controller IP

FPGA Family/ Speed Grade	Timing Mux	SRAM Clock Speed
Virtex-7 /-3 Kintex-7 /-3	2:1	600 MHz
	4:1	700 MHz

SigmaQuad-IVe Memory Controller IP

FPGA Family		Timing Mux	Operating Frequency
Xilinx	Virtex-UltraScale	2:1	Upto 725 MHz
	Kintex-UltraScale	4:1	TBD

Leading-Edge Memory Solutions for Xilinx & Altera FPGAs

a. GSI Technology customers now have access to a free Controller IP for our SigmaQuad-II+TM, SigmaQuad-IIIeTM, SigmaQuad-IVeTM SRAMs – Xilinx FPGA
b. Customer can access free SRAM Port IP for Altera Stratix – V FPGA
c. SigmaQuad-II+TM - Controller IP Overview
- Utilizes a "2:1 Mux" configuration for max performance: SRAM clock = 2x FPGA User Interface clock
- Read Latency = ~15 FPGA User Interface clock cycles (2:1 Mux)
- Validated by GSI on a KU040 evaluation board

d. SigmaQuad-IIIeTM & SigmaQuad-IVeTM - Controller IP Overview
- Utilizes a "4:1 Mux" configuration for max performance: SRAM clock = 4xFPGA User Interface clock; "2:1 Mux" configuration is also available for slower speeds
- Read Latency = ~15 FPGA User Interface clock cycles (4:1 Mux)
- Validated by GSI on a KU040 evaluation board

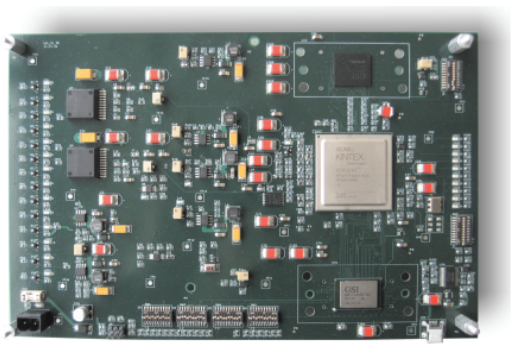
Engagement Process

- Review, or assist in creating, customer FPGA —> SRAM pinout
- Provide IP source code for simulation**, along with SRAM behaviour model
- Provide IP source code for synthesis**/P&R/FPGA build

(**Note: IP source code is typically the same for simulation and for synthesis.)

Available Deliverables

- Controller IP Source Code (unencrypted Verilog)
- Design Constraints File
- Controller IP User Guide
- SRAM Behavioural Models, for simulation



Technical Notes

Timing Designer

SigmaQuad-IIIe Memory Controller IP

FPGA Family		Timing Mux	Operating Frequency
Xilinx	Virtex-6	2:1	Upto 500 MHz
	Virtex-7	2:1	Upto 600 MHz
	Kintex-7	4:1	Upto 800 MHz
	Virtex-UltraScale	2:1	Upto 725 MHz
	Kintex-UltraScale	4:1	TBD
Altera	Stratix-V	2:1	Up to 700 MHz

NEXCOMM asia

Nexcomm Asia Pte Ltd
13 Braddell Tech, #06-04,
Toa Payoh, Lorong 8, Singapore 319261
Tel: +65 6891 2335
Fax: +65 6766 8117

nxm-enquiry@nexcomm-asia.com

www.nexcomm-asia.com

Bengaluru
M: +91 80 4203 2277

Hyderabad
M : +91 99639 92277

Delhi
M: +91 95912 31147

Pune
M: +91 88056 66002

Malaysia
Tel: +03 7652 2813

Indonesia
Tel: +6221 2934 9381

Soho Mayanmar
Tel: 09 400467496

China
Tel: +86 13923 707318

Soho Vietnam
HP: 0905474745