NEXCOMM asia

GSI TECHNOLOGY

Founded in 1995, GSI Technology, Inc. is a leading provider of high performance semiconductor memory solutions for military, medical, automotive and other applications.
"SigmaDDR SRAMs are synchronous memories with a common read and write data bus. "DDR" refers to their ability to transfer 2 beats of data on the data bus in a single clock cycle"

Military Temperature SigmaDDR SRAMs

SigmaDDR-IVe™ SRAMs

144Mb SigmaDDR-IVe (Package - 260 BGA)

GSI P/N	Config	Speed (MHz)	Voltage	Features
GS81314LT36GK-120M GS81314LT18GK-120M	4M x 36 8M x 18	1200	V_{DD}—1.25 ~ 1.3 V V_{DDQ}—1.2 ~ 1.3 V HSTL I/O	SigmaDDR-IVe Burst of 2 Read Latency = 6 On-Die Termination Option Multi-Bank, ECCRAM™
GS81314LT37GK-800M GS81314LT19GK-800M	4M x 36 8M x 18	800	V_{DD}—1.25 ~ 1.3 V V_{DDQ}—1.2 ~ 1.3 V HSTL I/O	SigmaDDR-IVe Burst of 2 Read Latency = 6 On-Die Termination Option Multi-Bank, ECCRAM™

SigmaDDR-IIIe™ SRAMs

288Mb SigmaDDR-IIIe (Package - 260 BGA)

GSI P/N	Config	Speed (MHz)	Voltage	Features
GS82583ET36GK-625M GS82583ET18GK-625M	8M x 36 16M x 18	625	V_{DD}—1.25 ~ 1.3 V V_{DDQ}—1.2 ~ 1.3 V 1.5 V	DDR-IIIe Burst of 2 Read Latency = 3 On-Die Termination Option

144Mb SigmaDDR-IIIe (Package - 260 BGA)

GSI P/N	Config	Speed (MHz)	Voltage	Features
GS81313LT36GK-714M GS81313LT18GK-714M	4M x 36 8M x 18	714	V_{DD}—1.25 ~ 1.3 V V_{DDQ}—1.2 ~ 1.3 V HSTL I/O	DDR-IIIe Burst of 2 Read Latency = 3 On-Die Termination Option ECCRAM™

72Mb SigmaDDR-IIIe (Package - 260 BGA)

GSI P/N	Config	Speed (MHz)	Voltage	Features
GS8673ET36BK-625M GS8673ET18BK-625M	2M x 36 4M x 18	625	V_{DD}—1.35 V V_{DDQ}—1.2 V/1.5 V	DDR-IIIe Burst of 2 Read Latency = 3 On-Die Termination Option ECCRAM™

SigmaDDR-II™ and SigmaDDR-II+™ SRAMs

144Mb SigmaDDR-II+ (Package - 165 BGA (15 x 17 mm)

GSI P/N	Config	Speed (MHz)	Voltage	Features
GS81302T38E-450M GS81302T20E-450M GS81302T11E-450M GS81302T06E-450M	4M x 36 8M x 18 16M x 9 16M x 8	450	V_{DD}—1.8 V V_{DDQ}—1.5 V/1.8 V	DDR-II+ Burst of 2 Read Latency = 2.5 On-Die Termination Option

144Mb SigmaDDR-II (Package - 165 BGA (15 x 17 mm)

GSI P/N	Config	Speed (MHz)	Voltage	Features
GS81302T36E-350M GS81302T18E-350M GS81302T09E-350M GS81302T08E-350M	4M x 36 8M x 18 16M x 9 16M x 8	350	V_{DD}—1.8 V V_{DDQ}—1.5 V/1.8 V	DDR-II+ Burst of 2

72Mb SigmaDDR-II+ (Package - 165 BGA (13 x 15 mm)

GSI P/N	Config	Speed (MHz)	Voltage	Features
GS8662T38BD-450M GS8662T20BD-450M GS8662T11BD-450M GS8662T06BD-450M	2M x 36 4M x 18 8M x 9 8M x 8	450	V_{DD}—1.8 V V_{DDQ}—1.5 V/1.8 V	DDR-II+ Burst of 2 Read Latency = 2.5

72Mb SigmaDDR-II (Package - 165 BGA (13 x 15 mm)

GSI P/N	Config	Speed (MHz)	Voltage	Features
GS8662T36BD-350M GS8662T18BD-350M GS8662T09BD-350M GS8662T08BD-350M	2M x 36 4M x 18 8M x 9 8M x 8	350	V_{DD}—1.8 V V_{DDQ}—1.5 V/1.8 V	DDR-II+ Burst of 2

36Mb SigmaDDR-II+ (Package - 165 BGA (13 x 15 mm)

GSI P/N	Config	Speed (MHz)	Voltage	Features
GS8342T38BD-500M GS8342T20BD-500M GS8342T11BD-500M GS8342T06BD-500M	1M x 36 2M x 18 4M x 9 4M x 8	500	V_{DD}—1.8 V V_{DDQ}—1.5 V/1.8 V	DDR-II+ Burst of 2 Read Latency = 2.5 On-Die Termination Option

36Mb SigmaDDR-II (Package - 165 BGA (13 x 15 mm)

GSI P/N	Config	Speed (MHz)	Voltage	Features
GS8342T36BD-350M GS8342T18BD-350M GS8342T09BD-350M GS8342T08BD-350M	1M x 36 2M x 18 4M x 9 4M x 8	350	V_{DD}—1.8 V V_{DDQ}—1.5 V/1.8 V	DDR-II Burst of 2

18Mb SigmaDDR-II+ (Package - 165 BGA (13 x 15 mm)

GSI P/N	Config	Speed (MHz)	Voltage	Features
GS8182T37BD-400M GS8182T19BD-400M	512K x 36 1M x 18	400	V_{DD}—1.8 V V_{DDQ}—1.5 V/1.8 V	DDR-II Burst of 2 Read Latency = 2.0

18Mb SigmaDDR-II (Package - 165 BGA (13 x 15 mm)

GSI P/N	Config	Speed (MHz)	Voltage	Features
GS8182T36BD-375M GS8182T18BD-375M GS8182T09BD-375M GS8182T08BD-375M	512K x 36 1M x 18 2M x 9 2M x 8	375	V_{DD}—1.8 V V_{DDQ}—1.5 V/1.8 V	DDR-II Burst of 2

SigmaDDR-II/II+ SRAMs

Desc.	Burst Size	Read Latency	Ordering Information				
			18Mb	36Mb	72Mb	144Mb	288Mb
Double Data Rate (CIO)	2		GS8182T	GS8342T	GS8662T GS8672T*	GS81302T	GS82582T
	4	1.5	GS8182R	GS8342R	GS8662R	GS81302R	GS82582R
Double Data Rate (SIO)	2	1.5	GS8182S	GS8342S	GS8662S	GS81302S	GS82582S

SigmaDDR-IIIe SRAMs

Interface	Burst Size	Read Latency	Operating Frequency	Ordering Information		
				72Mb (x18, x36)	144Mb (x18, x36)	288Mb (x18, x36)
Double Data Rate	2	3	Up to 725 MHz	GS8673ET	GS81313LT GS81313HT	GS82583ET

SigmaDDR-IVe SRAMs

Interface	Burst Size	Read Latency	Operating Frequency	Ordering Information
				144Mb (x18, x36)
Double Data Rate	2	6	Up to 1333 MHz	GS81314LT GS81314PT

SigmaDDR-II+ Memory Controller IP

FPGA Family/ Speed Grade	Timing Mux	SRAM Clock Speed
Virtex-7/-3 Kintex-7/-3	2:1	600 MHz
	4:1	700 MHz

Leading-Edge Memory Solutions for Xilinx & Altera FPGAs

a. Controller IP Overview - SigmaDDR-IIIe
- Utilizes a "4:1 Mux" configuration for max performance: SRAM clock = 4x FPGA User Interface clock; "2:1 Mux" configuration is also available for slower speeds
- Validated by GSI on a 7K325T evaluation board

b. Controller IP Overview - SigmaDDR-II+
- Utilizes a "4:1 Mux" configuration for max performance: SRAM clock = 4x FPGA User Interface clock; "2:1 Mux" configuration is also available for slower speeds
- Validated by GSI on Xilinx 7K325T evaluation board & Intel / Altera Stratix-V FPGA (2:1 Mux)

Engagement Process

- Review, or assist in creating, customer FPGA —> SRAM pinout
- Provide IP source code for simulation**, along with SRAM behaviour model
- Provide IP source code for synthesis**/P&R/FPGA build

Available Deliverables

- Controller IP Source Code (unencrypted Verilog)
- Design Constraints File
- Controller IP User Guide
- SRAM Behavioural Models, for simulation

Design Models

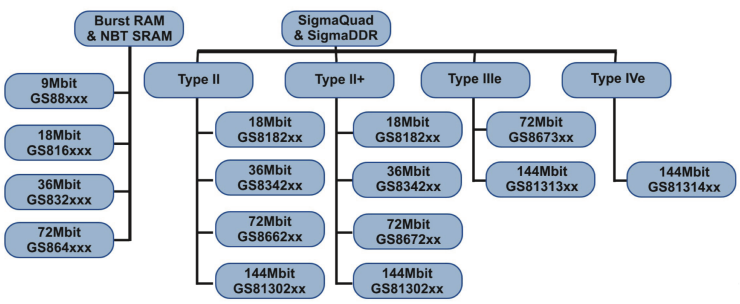
Verilog
- Configurable for full- or reduced-array simulations
- Error checks for proper timing constraints
- No compiler switches necessary for setup

VHDL
- Configured for worst-case data valid windows
- Configured for worst-case QK to data valid.

IBIS
- 100 data points for V/T and DC curves
- 50 data points for Power & Ground clamps
- Programmable-impedance I/Os: full range, 5Ω increments
- Programmable-termination inputs: full range, 5Ω increments
- Includes per-pin and mutual-per-pin RLC models

BSDL

Boundary-scan description language – available as needed



SigmaDDR-IIIe Memory Controller IP

FPGA Family		Timing Mux	Operating Frequency
Xilinx	Virtex-6	2:1	Up to 500 MHz
	Virtex- 7 Kintex-7	2:1	Up to 600 MHz
		4:1	Up to 800 MHz
	Virtex- UltraScale Kintex-UltraScale	2:1	Up to 725 MHz
		4:1	TBD
Altera	Stratix-V	2:1	Up to 700 MHz
	Arria-10		Forthcoming in 2016

Technical Notes

Timing Designer

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